

PATENT APPLICATION  
DOCKET NO.: 200209002-1

**LISTING OF THE CLAIMS**

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims of the present patent application.

1. (Original) A match circuit for implementation in a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the match circuit comprising logic for activating a match signal when a selected  $N$ -bit portion of the debug data matches an  $N$ -bit threshold for all bits selected by an  $N$ -bit match mask ("mmask").

2. (Original) The match circuit of claim 1 wherein  $N$  is equal to sixteen.

3. (Original) The match circuit of claim 1 wherein the  $N$ -bit threshold is provided from a control status register ("CSR").

4. (Original) The match circuit of claim 1 wherein the  $N$ -bit mmask is provided from a control status register ("CSR").

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5. (Original) The match circuit of claim 1 wherein the debug data comprises 80 bits.

6. (Original) The match circuit of claim 5 wherein the debug data comprises eight 16-bit portions aligned on 10-bit blocks.

7. (Original) The match circuit of claim 6 wherein the selected portion comprises one of the eight 16-bit portions.

8. (Original) The match circuit of claim 1 wherein the logic for activating a match signal comprises logic for comparing a binary bit of the selected debug data portion with a corresponding bit of the threshold and outputting a binary bit indicative of whether the compared bits match.

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9. (Original) Circuitry for implementation in a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the circuitry for analyzing a selected portion of the debug data, comprising:

logic means for activating a match signal when the selected portion of the debug data includes a specified bit pattern;

logic means for activating a threshold signal based on a comparison between at least a subset of the selected debug data portion and a threshold value; and

logic means for outputting one of the match signal and the threshold signal in response to a selection control signal.

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10. (Original) The circuitry of claim 9 wherein the logic means for activating a match signal further comprises:

an exclusive NOR ("XNOR") circuit operating to perform a bit-wise XNOR operation between the selected debug data portion and a threshold register that is as wide as the selected debug data portion;

an OR circuit for ORing an inverted mask ("mmask") with the output of the XNOR circuit; and

an AND circuit operating to AND the OR circuit's output to generate the match signal.

11. (Original) The circuitry of claim 10 wherein the mmask is provided from a control status register ("CSR").

12. (Original) The circuitry of claim 10 wherein the threshold register is provided as a control status register ("CSR").

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13. (Original) The circuitry of claim 10 wherein the debug data comprises 80 bits.

14. (Original) The circuitry of claim 10 wherein the debug data comprises eight 16-bit portions aligned on 10-bit blocks.

15. (Original) The circuitry of claim 14 wherein the selected portion comprises one of the eight 16-bit portions.

16. (Original) The circuitry of claim 9 wherein the logic means for activating a threshold signal comprises a compare circuit that outputs a logic one when the subset of the selected debug data portion is greater than or equal to the threshold value.

17. (Original) The circuitry of claim 9 wherein the logic means for outputting one of the match signal and the threshold signal comprises a 2:1 multiplexer circuit.



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18. (Original) A method operable in a general purpose performance counter ("GPPEC") connected to a bus carrying debug data for of analyzing a selected portion of the debug data, the method comprising:

activating a match signal when the selected portion of the debug data includes a specified bit pattern;

activating a threshold signal based on a comparison between at least a subset of the selected debug data portion and a threshold value; and

outputting one of the match signal and the threshold signal in response to a selection control signal.

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19. (Original) The method of claim 18 wherein the activating of a match signal comprises:

performing a bit-wise exclusive NOR operation between the selected debug data portion and a threshold register that is as wide as the selected debug data portion to create a first intermediary output;

performing an OR operation between the first intermediary output and an inverted mask ("mmask") to create a second intermediary output; and

performing an AND operation on the second intermediary output to generate the match signal.

20. (Original) The method of claim 19 wherein the mmask is provided from a control status register ("CSR").

21. (Original) The method of claim 19 wherein the threshold value is provided from a control status register ("CSR") operating as the threshold register.



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22. (Original) The method of claim 19 wherein the selected portion of the debug data comprises 16 bits.

23. (Original) The method of claim 19 wherein the debug data comprises eight 16-bit portions aligned on 10-bit blocks.

24. (Original) The method of claim 23 wherein the selected portion comprises one of the eight 16-bit portions.

25. (Original) The method of claim 18 wherein the activating of a threshold signal comprises outputting a logic one when the subset of the selected debug data portion is greater than or equal to the threshold value.